

# 1-Page OPN Decoder

Cyclone V FPGA

*Updated 11 April 2013*

# Cyclone V FPGA Feature-Based Ordering Codes

Example Ordering Code: **5CGXFC7D6F31C6N**

		Package Code (Pin Count)	M11 (301)	M13 (383)	M15 (484)	U15 (324)	U19 (484)	F17 (256)	F23 (484)	F27 (672)	F31 (896)	F35 (1152)											
		Transceiver Count	F 4	- 0	C 6	- 0	B 3	- 0	B 3	A 5	C 6	- 0	- 0	B 3	C 6	- 0	C 6	D 9	- 0	D 9	E 12	E 12	
GX	Hard IP	Base (B) HMC, PCIe = 0, 0				C7		C3		C3	C9	C4 C5 C7 C9			C3	C4 C5 C7 C9		C4 C5	C7 C9		C7	C9	C9
		Full (F) HMC, PCIe = 1, 1 HMC, PCIe = 2, 2 HMC, PCIe = 2, 1 HMC, PCIe = 0, 1	C4 C5		C4 C5	C7		C3		C3	C9	C4 C5 C7 C9			C3	C4 C5 C7 C9		C4 C5	C7 C9		C7	C9	C9
Full (F) HMC, PCIe = 1, 1 HMC, PCIe = 2, 2 HMC, PCIe = 2, 1 HMC, PCIe = 0, 1		D5		D5	D7			D9	D5 D7			D5 D7 D9				D5 D7 D9		D5	D7 D9		D7	D9	D9
E		Base (B) HMC, PCIe = 0, 0				A7		A2 A4		A2 A4 A5 A7 A9			A2 A4 A5 A7 A9				A7 A9				A7 A9		
		Full (F) HMC, PCIe = 1, 0 HMC, PCIe = 2, 0		A2 A4 A5		A7			A2 A4 A5 A7 A9					A2 A4 A5 A7 A9			A7 A9				A7 A9		

**5CGX**   **F**   **C**   **7**   **D**   **6**   **F31**   **C**   **6**   **X**   **N**

Family Variant	Hard IP (HMC, PCle)	Product Line	Density (in KLEs)	XCVR Count	XCVR Speed	Package	Temperature Grades	Device Speed Grade	Optional Suffix	Optional Suffix
<b>E</b> = logic only <b>GX</b> = 3G XCVR <b>GT</b> = 6G XCVR  <b>Note:</b> • Automotive Grade GT comes with 5G XCVR.	<b>B</b> = Base (0, 0) <b>F</b> = Full (1, 1), (2, 2), (2, 1) or (0, 1)	<b>A</b> = E <b>C</b> = GX <b>D</b> = GT	<b>A2</b> = 25 <b>A4</b> = 48 <b>A5</b> = 76.5 <b>A7</b> = 149.5 <b>A9</b> = 301 <b>C3</b> = 31 <b>C4</b> = 50 <b>C5</b> = 76.5 <b>C7</b> = 149.5 <b>C9</b> = 301 <b>D5</b> = 76.5 <b>D7</b> = 149.5 <b>D9</b> = 301	<b>A</b> = 5 <b>B</b> = 3 <b>C</b> = 6 <b>D</b> = 9 <b>E</b> = 12 <b>F</b> = 4  <b>Notes:</b> • Omit for E devices. • For Automotive Grade devices, the value of XCVR speed 5 is 5.0G.	<b>5</b> = 6.144G <b>6</b> = 3.125G <b>7</b> = 2.5G  <b>Notes:</b> • Omit for E devices. • XCVR speed 5 is only offered for GT devices. • For Automotive Grade devices, the value of XCVR speed 5 is 5.0G.	<b>Ball Pitch</b> <b>M</b> = 0.5mm <b>U</b> = 0.8mm <b>F</b> = 1.0mm  <b>Size (mm<sup>2</sup>)</b> <b>M:</b> 11, 13, 15 <b>U:</b> 15, 19 <b>F:</b> 17, 23, 27, 31, 35	<b>C</b> = Commercial <b>I</b> = Industrial <b>A</b> = Automotive  <b>Notes:</b> • I & A offered in mid device and XCVR speed grade only. • A grades offered for limited packages only. Contact factory.	<b>6</b> = Fast <b>7</b> = Mid <b>8</b> = Slow  <b>Notes:</b> • 400 MHz DRAM in fast speed grade only, otherwise 333MHz.	Reserved	<b>N</b> = lead free <b>ES</b> = eng. sample <b>NES</b> = lead free, eng. sample

# Cyclone V SoC FPGA Feature-Based Ordering Codes

Example Ordering Code: **5CSTFD6D5F31C6ES**

	Package (pins) FPGA IO / HPS IO	U19 (484) 66 / 161		U23 (672) 124 / 188		F31 (896) 288 / 188	
	Transceiver Count (# , speed)	- (0, 0)		- (0, 0)    C (6, 3G)		- (0, 0)    D (9, 3G)    D (9, 5G)	
Hard IP	<b>Base (B)</b> FPGA Hard Memory Controller (HMC) = 0 * PCIe = 0 Single core option **	A2 A4		A2 A4 A5 A6			
	<b>Mid (M)</b> FPGA HMC = 1 * PCIe = 0	A5 A6		A5 A6		A5 A6    C5 C6	
	<b>Full (F)</b> FPGA HMC = 1 * PCIe = 2			C4 C5 C6		C5 C6    D5 D6	

**5CST**

**F**

**D**

**6**

**D**

**5**

**F31**

**I**

**6**

**S**

**ES**

**Family  
Variant**

5CSE = logic only  
5CSX = 3G XCVR  
5CST = 5G XCVR

**Hard IP  
(HMC,PCIe)**

B = Base (0,0)  
M = Mid (1,0)  
F = Full (1,2)

**Notes:**

\* Value does not include the HMC in the Hard Processor System (HPS).

\*\* Single core in "Base" configuration, C and A temp grades only

**Product  
Line**

A = SE  
C = SX  
D = ST

**Density  
(in KLEs)**

2 = 25  
4 = 40  
5 = 85  
6 = 110

**XCVR  
Count**

C = 6  
D = 9

**Note:**  
• Omit for SE devices

**XCVR  
Speed  
(Gbps)**

5 = 5.0G  
6 = 3.125G

**Notes:**  
• Omit for SE devices  
• 6G XCVR not available in slow device speed grade.

**Package**

Ball Pitch  
U = 0.8mm  
F = 1.0mm

**Package  
Size (mm<sup>2</sup>)**

19  
23  
31

**Temperature  
Grades**

C = Commercial  
I = Industrial \*  
A = Automotive \*

**Notes:**

\* I & A in mid device speed grade only.

\* CAN controller in I & A temp grades only.

**Device  
Speed  
Grade**

6 = Fast  
7 = Mid  
8 = Slow

**Note:**

• 400 MHz DRAM in fast speed grade only, otherwise 333MHz

**Optional  
Single Core**

S = single core  
Omit for dual core

**Note:**

• Single core in "Base" Hard IP configuration, C and A temp grades only

**Optional  
Suffix**

N = lead free

ES = Eng. Sample

NES – lead free, eng. sample