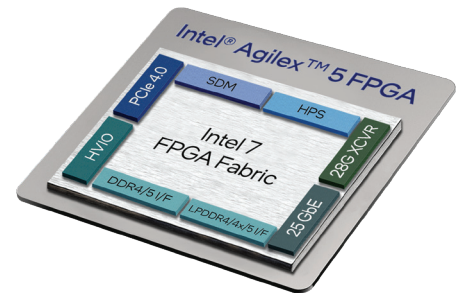


Intel® Agilex™ 5 FPGAs and SoCs

Midrange FPGAs optimized for high performance, lower power, and smaller form factors



Extending the innovations of Intel® Agilex™ devices to midrange FPGA applications, Intel® Agilex™ 5 devices serve a broad range of applications that require high performance, lower power, smaller form factors and lower logic densities.

Intel Agilex 5 devices also feature the industry's first Enhanced DSP with AI Tensor Block, which deliver high-efficiency artificial intelligence (AI) and digital signal processing (DSP) functionality, and the FPGA industry's first asymmetric applications processor system consisting of dual Arm Cortex-A76 cores and dual Cortex-A55 cores, which enable you to optimize the performance and power efficiency of their workloads.

In addition to that, built using Intel 7 technology, Intel Agilex 5 FPGAs offer advanced features such as a second-generation Intel® Hyperflex™ FPGA Architecture, high-speed transceivers support up to 28.1 Gbps, and PCIe 4.0 x8, DDR memory interface up to DDR5 at 4,000 Mbps, and general purpose I/O from 1.05 V to 3.3 V. These characteristics make them ideal for midrange FPGA applications across the edge and core including wireless and wireline communications, video and broadcast equipment, industrial applications, test and measurement products, medical electronics, data center and defense applications.

Up to
2X
better fabric
performance/watt
D-Series FPGAs vs
competing 7 nm FPGAs

2.5X
Higher Performance ^{1,3†}

50%
Lower Power ^{1,3†}

37X
Peak INT8 TOPS ^{1,2,3†}

Intel Agilex 5 FPGAs Focus Markets

Industrial

- Camera interface
- IoT 4.0 gateway
- Industrial drives
- Robot controller (Cell, Motion)
- PLC
- IoT 4.0 edge compute

Broadcast/Medical

- Interactive white board (IWB)
- AV networking
- Cameras, 8K Video
- Video conferencing
- Ultrasound, X-ray, MRI, endo/ laparoscope

Wireline/Wireless

- Sidecar board controller
- Control OTN
- I/O bridging
- Macro cells
- Radio units
- xHaul

Test/Measurement/Retail

- Display Automatic Test Equipment
- Terminal devices (Parking meters, lighting, environmental sensors)
- Multi-camera
- Video analytics

Defense

- Secure communications
- Avionics
- Aerospace systems

Data Center

- Infrastructure acceleration
- Application acceleration

This tier consists of the performance-optimized D-Series FPGAs, and the power-optimized E-Series FPGAs. D-Series FPGAs deliver up to ~1.5X better fabric performance while consuming ~42% lower total power compared to Intel® Stratix® 10 FPGAs. For more power-sensitive applications, the E-Series FPGAs consume ~50% lower power while delivering ~2.5X better performance than prior generation edge centric devices of Cyclone® V devices.

Intel Agilex 5 FPGA Series		
	E-Series	D-Series
	Optimized for power and size – Ideal for intelligent applications at the edge, embedded and more	Optimized for performance and power efficiency – Ideal for various applications across multiple markets
Logic Density	50K – 656K LEs	100K – 644K LEs
Package Size	As small as 15mm x 15mm	As small as 23mm x 23mm
Power Comparison	50% lower vs Cyclone V FPGA	42% lower vs Intel Stratix 10 FPGA
Fabric Performance	2.5X vs Cyclone V FPGA	1.5X vs Intel Stratix 10 FPGA
Max Transceiver Rate	24 x 17 Gbps / 28 Gbps	32 x 28 Gbps
Max PCIe and GbE Rate	PCIe 4.0 x4 and 10/25GbE x6	PCIe 4.0 x8 and 25GbE x16
Max External Memory Interface Data Rate	DDR5 @ 3,600 Mbps, DDR4 @ 2,667 Mbps, LPDDR4/5 @ 3,733 Mbps	DDR5 @ 4,000 Mbps, DDR4 @ 3,200 Mbps, LPDDR4/4x/5 @ 4,267 Mbps, QDR IV @ 2,132 Mbps
Peak TOPS INT8	26	56
Max DSP 18x19 Multipliers	1,692	3,680
Fabric Speed	350 MHz / 500 MHz	600 MHz
Hard Processor System	Multi-core Arm Processors of Dual-core A55 @ 1.5 GHz and Dual-core A76 @ 1.8 GHz	
MIPI	D-PHY v2.5 at up to 3.5 Gbps ⁴ per lane	



Intel Agilex 5 FPGAs and SoCs – Key Innovations

Key Innovations ⁵	
Manufactured using advanced Intel technologies and processes	Utilizes advanced Intel process technologies (Intel 7), contributing to high performance, power efficiency, and supply chain resiliency
2nd generation Intel Hyperflex FPGA Architecture	Enables significant design optimization to deliver up to 2.5X higher performance, or up to 50% lower total power compared with Cyclone V FPGAs. [†]
Transceiver data rates	Supports up to 32 x 28 Gbps data rates for data intensive applications and hardened media access control, physical coding sublayer (PCS), and forward error correction (FEC) up to 16 x 25 Gbps Ethernet (GbE) for networking applications.
Hardened PCI Express (PCIe) support	Up to PCIe 4.0 x8 interface
Advanced memory interface support	Support industry standard DDR4, DDR5, LPDDR4, and LPDDR5
Hardened processors	Multi-core Arm processors of dual-core of A55 (up to 1.5 GHz) and dual-core of A76 (up to 1.8 GHz)
AI Tensor Block	AI Tensor Block has up to 37X ¹ peak theoretical TOPS improvement in INT8 operations versus Cyclone V FPGAs
MIPI support	MIPI D-PHY v2.5 at up to 3.5 ⁴ Gbps per lane

For More Information

- Intel Agilex FPGAs and SoC FPGAs portfolio page: [intel.com/agilex](https://www.intel.com/agilex)
- Intel Agilex 5 FPGAs and SoC FPGAs product page: [intel.com/agilex5](https://www.intel.com/agilex5)
- Intel Agilex 5 FPGA and SoC FPGA White Paper: [intel.com/agilex5-wp](https://www.intel.com/agilex5-wp)
- Intel® Quartus® Prime Software page: [intel.com/quartus](https://www.intel.com/quartus)
- Contact an Intel sales representative for inquiries



¹ Comparing E-Series FPGAs with Cyclone® V FPGAs

² With INT8 TOPS configuration

³ Based on current estimates

⁴ Up to 3.5 Gbps for standard reference channel, and up to 2.5 Gbps for long reference channel

⁵ The key innovations are different for each Intel Agilex 5 FPGA series

[†] Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance.

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