AN 793: Intel® Arria® 10 DisplayPort 4Kp60 with Video and Image Processing Pipeline Retransmit Reference Design

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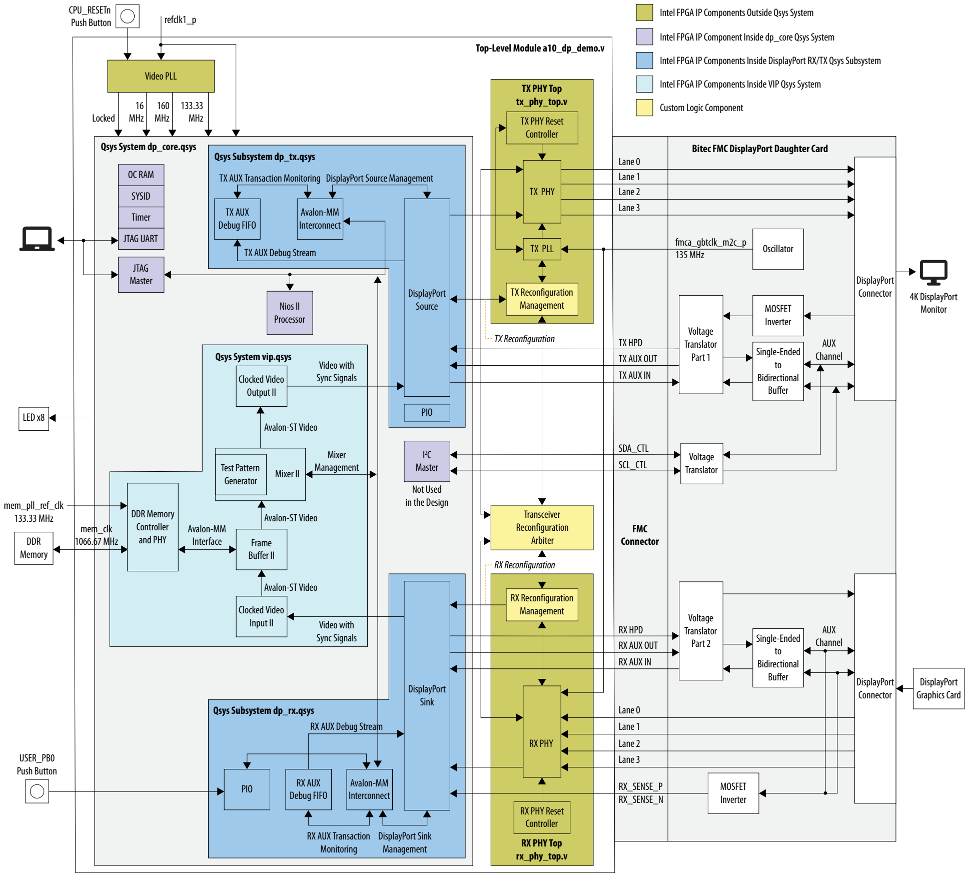
Contents

Arria® 10 DisplayPort 4Kp60 with Video and Image Processing Pipeline Retransmit Reference Design

The Arria® 10 DisplayPort 4Kp60 with Video and Image Processing Pipeline Retransmit reference design demonstrates Intel's video connectivity, the DisplayPort Sink (RX) and Source (TX) functions using a video loop-through system.

Figure 1. Reference Design Block Diagram



1. The reference design receives video data (up to a resolution of 3840 pixels × 2160 lines) over the DisplayPort RX link.
2. The design then converts the received video to Avalon Streaming (Avalon-ST) image stream and stores into the external memory.
3. The design mixes the buffered image with a 3840 × 2160 color bar background and sends the combined image to the DisplayPort Source.
4. The DisplayPort Source transmits the combined image to a DisplayPort capable monitor over the DisplayPort TX link.
5. The DisplayPort interface supports dynamic scaling between 1, 2 and 4 lanes:
    - Reduced Bit Rate (RBR) @ 1.62 Gbps/lane
    - High Bit Rate (HBR) @ 2.7 Gbps/lane
    - High Bit Rate 2 (HBR2) @ 5.4 Gbps/lane

    The TX and RX physical layer (PHY) are independent of each other although they are placed at the same transceiver channels; the DisplayPort Sink may run at 1 lane @ 2.7 Gbps while the DisplayPort Source runs at 4 lanes @ 5.4 Gbps concurrently. There is no audio or secondary stream being retransmitted in this reference design.

    This reference design is implemented using Intel's Qsys integration tool and standalone HDL modules.

Note: The I^{2}C interface is not used in this design.

Related Information

- DisplayPort IP Core User Guide
- Video and Image Processing Suite User Guide
- Arria 10 DisplayPort 4Kp60 with Video and Image Processing Pipeline Retransmit Reference Design (Quartus Prime Pro Edition)
  Click to get the reference design files using the Quartus Prime 17.0 Pro Edition software. Click on the tabs for other versions.
- Arria 10 DisplayPort 4Kp60 with Video and Image Processing Pipeline Retransmit Reference Design (Quartus Prime Standard Edition)
  Click to get the reference design files using the Quartus Prime 17.0 Standard Edition software. Click on the tabs for other versions.
- Arria 10 GX FPGA Development Kit
  Refer to this page for more information about the Arria 10 GX FPGA Development Kit.
- FMC DisplayPort Daughter Card

Reference Design Components

The reference design consists of Qsys, PHY, and Clock subsystems.

Table 1. Reference Design Components

The table lists the major components in the reference design.

System	Components
Qsys subsystem	DisplayPort Source and Sink cores
	Video and Image Processing IP cores • Clocked Video Input II (CVI) • Clocked Video Output II (CVO) • Frame Buffer II • Mixer II
	Nios II processor
	DDR4 External Memory Interface
	Avalon Memory-Mapped (Avalon-MM) FIFO Memory
	JTAG to Avalon-MM master bridge
PHY subsystem	Simplex TX and RX Native PHY
	TX fPLL
	Intel® Transceiver PHY Reset Controller
	TX and RX Bitec reconfiguration module
	Transceiver reconfiguration arbiter
Clock subsystem	IO PLL for video data path

Clocking Scheme

The reference design requires several clock sources from the FPGA development kit and the FMC daughter card for proper operation. The reference design uses the default clock frequency from the oscillator; no programming is required through the Clock Control application.

Table 2. Clock Signals

Signal	Description	Pin Number	I/O Standard	Usage
`refclk1_p`	External 100 MHz clock from X3 programmable oscillator on the FPGA development kit.	AG37/AG38	LVDS	• Avalon-MM interface for DisplayPort and VIP IP cores • Transceiver reconfiguration interface • TX and RX Bitec reconfiguration management • Transceiver reconfiguration arbiter • Intel PHY reset controller • TX PLL and TX/RX transceiver channel reconfiguration interfaces • Nios II CPU and peripherals • Video PLL (IO PLL) input reference clock
`fmca_gbtclk_m2c_p`	External 135 MHz clock from Bitec FMC daughter card. The oscillator is not programmable.	AL8/AL7	LVDS	• TX PLL input reference clock • RX CDR input reference clock

continued...

Signal	Description	Pin Number	I/O Standard	Usage
`mem_pll_ref_clk`	External 133 MHz clock from U26 programmable oscillator on the FPGA development kit.	F34/F35	LVDS	DDR4 external memory interface input reference clock
`dp_tx_vid_clk`	Generated 133.33 MHz clock from video PLL.		–	DisplayPort Source–Clocked Video Output interface
`dp_rx_vid_clk`	Generated 160 MHz clock from video PLL.	–	–	• DisplayPort Sink–Clocked Video Output interface • Avalon-ST video data path
`clk_16`	Generated 16MHz clock from video PLL	–	–	• DisplayPort Sink and Source 1 Mbps AUX channel interface • DisplayPort Sink and Source AUX debug FIFO
`clk_cal`	Derived 50MHz clock from refclk1	–	–	DisplayPort Sink and Source calibration. This clock must be synchronous to the clock used for the transceiver reconfiguration block (100 MHz)

The 160 MHz clock output from the video PLL drives the DisplayPort Sink and Clocked Video Input interface. This interface runs at input video pixel clock domain; this clock frequency must be equal or greater than the required pixel clock frequency of the input video stream.

Note: The ANSI/CEA-861-F standard requires the 3840 × 2160 @ 60 Hz video stream to run at 594.0 MHz pixel clock. This design uses 4 pixels per clock so that the interface runs at 148.5 MHz (quarter rate of 594.0 MHz), but with 4 times video bus width between the DisplayPort Sink and Clocked Video Input. Because 160 MHz is higher than 148.5 MHz, this frequency is sufficient to support 4Kp60 input video stream.

The 133.33 MHz clock output from the video PLL drives the DisplayPort Source and Clocked Video Output interface. The CVT-RB specification states that the 133.33 MHz should be derived from the reduced blanking period of the 4K video output stream.

Table 3. 4Kp60 Video Stream Timing Information for Normal and Reduced Blanking

H Active × V Active	H Total	H Blank	V Total	V Blank	Pixel Frequency
Normal	4,400	560	2,250	90	594.00 MHz
Reduced	4,000	160	2,222	62	533.28 MHz

This design uses 4 pixels per clock so that the interface runs at 133.33 MHz (quarter rate of 533.28 MHz), but with 4 times wider video bus between the DisplayPort Source and Clocked Video Output.

DisplayPort IP Core

The reference design uses specific DisplayPort IP core parameter settings.

Table 4. DisplayPort IP Core Settings for the Reference Design

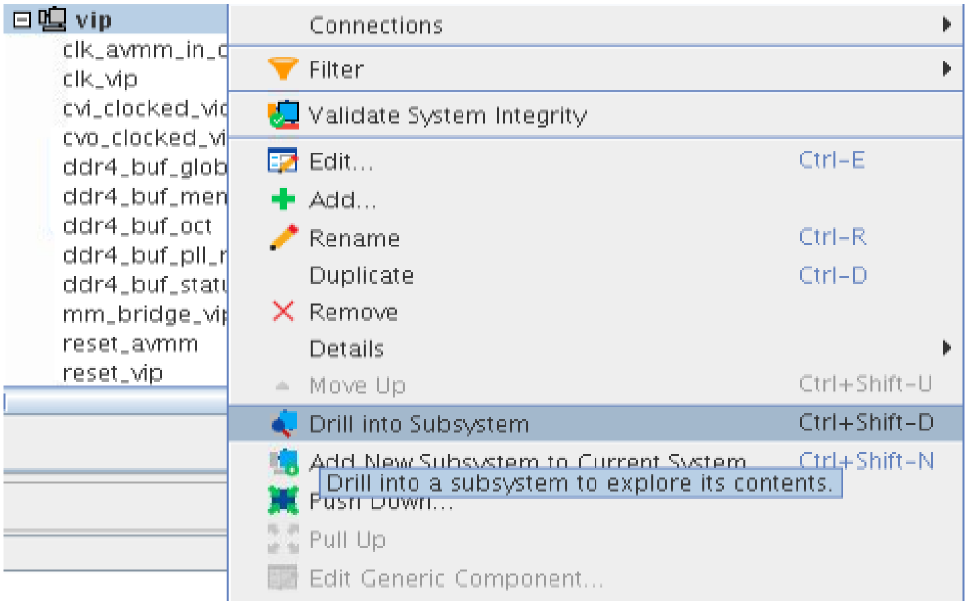
<table>
<tr><th>Parameter</th><th>Value</th><th>Notes</th></tr>
<tr><td><b>Maximum video input color depth (TX)</b> /
<b>Maximum video output color depth (RX)</b></td><td>10 bpc</td><td>This reference design supports GPU and monitor up to a maximum of 10 bit-per-color depth.</td></tr>
<tr><td><b>Maximum link rate</b></td><td>5.4 Gbps</td><td rowspan="2">The bandwidth requirement for 4Kp60, 10 bpc video stream through serial link:
Active video resolution = 3840 × 2160 pixels/frame
Total resolution (including reduced blanking) = 4000 × 2222 pixels/frame
Refresh rate = 60 Hz or 60 frames per second
Bits per pixel = 10 bpc × 3 colors = 30 bits per pixel
Total bandwidth = (4000 × 2222) pixel/frame × 60 frame/s × 30 bits/pixel = 15.9984 Gbits/s
With 8b/10b encoding scheme, the actual bandwidth required = 15.9984 × 10/8 = 19.998 Gbps
With 4 lanes at 5.4 Gbps, the aggregated bandwidth of 21.6 Gbps is sufficient to support the 4K video stream at 60 Hz refresh rate.</td></tr>
<tr><td><b>Maximum lane count</b></td><td>4</td></tr>
<tr><td><b>Symbol output mode (Source)</b> /
<b>Symbol input mode (Sink)</b></td><td>Dual</td><td>Symbol mode affects the transceiver parallel bus width and the DisplayPort IP core clock frequency. The DisplayPort IP core synchronizes with the transceiver parallel clock. The parallel clock frequency is link rate/transceiver parallel bus width.
The table below shows the frequency for HBR2 (5.4 Gbps).
<table>
<tr><th>Symbol Mode</th><th>Transceiver Recovered Clock</th></tr>
<tr><td>Dual (20 bits)</td><td>5400/20 = 270 MHz</td></tr>
<tr><td>Quad (40 bits)</td><td>5400/40 = 135 MHz</td></tr>
</table></td></tr>
<tr><td><b>Pixel input mode (Source)</b>/
<b>Pixel output mode (Sink)</b></td><td>Quad</td><td>Pixel mode affects the video clock frequency and video port width of the IP core.
For 4Kp60 video stream, the bandwidth requirement is 4000 × 2222 × 60 pixel/s = 533280000 pixels/s. Because of the high bandwidth requirement, the design requires dual or quad pixel mode for timing closure.
<table>
<tr><th>Pixel Mode</th><th>Video Clock</th></tr>
<tr><td>Single (1 pixel/clock)</td><td>533.28 MHz</td></tr>
<tr><td>Dual (2 pixels/clock)</td><td>266.64 MHz</td></tr>
<tr><td>Quad (4 pixels/clock)</td><td>133.32 MHz</td></tr>
</table></td></tr>
</table>

Video and Image Processing Block

The Video and Image Processing (VIP) block is a subsystem within the Qsys system in the design.

The VIP block receives video data from the DisplayPort Sink, processes and transmits the processed data to the DisplayPort Source. To navigate to the VIP subsystem through `dp_core.qsys`, right click **vip**, and select **Drill into subsystem**.

Figure 2. Navigating to the VIP Subsystem



The VIP block comprises the following components:

- Clocked Video Input II IP core: Converts the DisplayPort Sink video output format to Avalon-ST video protocol
- Frame Buffer II IP core: Handles mismatch in RX and TX video data rate through triple-buffering
- Mixer II IP core: Overlays the buffered image on top of the background color bar
- Clocked Video Output II IP core: Converts the Avalon-ST video protocol to the DisplayPort Source video input format

This reference design supports 4K resolution.

Table 5. VIP IP Core Settings for the Reference Design

IP Core	Parameter	Value
Clocked Video Input II	**Bits per pixel per color plane**	10
	Number of color planes	3
	Number of pixels in parallel	4
	Use control port	Off
Frame Buffer II	**Maximum frame width**	3840
	Maximum frame height	2160
	Bits per pixel per color plane	10
	Number of color planes	3
	Pixels in parallel	4
	Avalon-MM master (s) local ports width	512
	AV-MM burst target write	64

continued...

IP Core	Parameter	Value
	AV-MM burst target read	64
	Frame dropping	On
	Frame repeating	On
	Drop invalid frames	On
	Run-time writer control	Off
Mixer II	**Maximum output frame width**	3840
	Maximum output frame height	2160
	Bits per pixel per color plane	10
	Number of pixels in parallel	4
	Colorspace (used for background layer)	RGB
	Pattern	Color bars
	How user packets are handled	Discard all user packets received
Clocked Video Output II	**Image width / Active pixels**	3840
	Image height / Active lines	2160
	Bits per pixel per color plane	10
	Number of color planes	3
	Number of pixels in parallel	4
	Separate syncs only - Frame/ Field 1 Horizontal sync	32
	Separate syncs only - Frame/ Field 1 Horizontal front porch	48
	Separate syncs only - Frame/ Field 1 Horizontal back porch	80
	Separate syncs only - Frame/ Field 1 Vertical sync	5
	Separate syncs only - Frame/ Field 1 Vertical front porch	3
	Separate syncs only - Frame/ Field 1 Vertical back porch	54
	Pixel FIFO size	3840
	FIFO level at which to start output	3839
	Use control port	Off

External Memory Interface

The Frame Buffer II IP core uses the external SDRAM to triple-buffer video frames and handle mismatch in RX and TX video data rates.

The IP core writes to the memory to store input pixels and reads from the memory to retrieve video frames and transmit them. The Arria 10 FPGA Development Kit has a HiLo connector for the DDR4 module. The DDR4 module is part of the development kit. The module has x72 @ 1200 MHz interface.

The **Arria 10 GX FPGA Development Kit with DDR4 HiLo** preset applies to the External Memory Interface instance, except for DQ width set to 64. The Frame Buffer II IP core supports up to a DQ width of x64.

Nios II Processor

The DisplayPort Source and Sink require a processor (e.g. Nios II processor) to act as link policy maker.

The design requires the **Enable GPU Control** option for the DisplayPort Sink to be turned on.

The Nios II processor performs the following functions:

- Runs software that acts as a DisplayPort link policy maker.
- Provides access to the DisplayPort IP core status and debug registers.
- Retrieves AUX channel transaction logs from the DisplayPort Source and Sink AUX debug FIFO.
- Monitors push buttons to print Main Stream Attribute (MSA) values and AUX channel transaction logs to the Nios II terminal.
- Initializes the VIP Suite IP cores.

Transceiver

The DisplayPort main link uses the Native PHY IP core for serial communication between the GPU and monitor.

The reference design uses separate simplex TX and RX PHY blocks because the TX and RX channels may run at different data rates based on the link training results.

Table 6. Native PHY Parameter Settings

Parameter	Value	Corresponding DisplayPort Source/Sink Parameters
Number of data channels	4	Maximum lane count = 4
Data rate (Mbps)	5,400	TX/RX maximum link rate = 5.4 Gbps
Standard PCS/PMA interface width	20	Symbol input/output mode = Dual
TX/RX byte serializer mode	Disabled	

The design uses two Intel transceiver PHY reset controllers to control the TX and RX PHY blocks independently.

Note: The 70 µs delay is not applied to the transceiver PHY reset controllers because the delay is too long for the DisplayPort Source and Sink cores to complete the link training. Instead, the design uses the acknowledgment model.

The Bitec reconfiguration management module controls the reset input of the PHY reset controllers, and manages the dynamic reconfiguration of the TX PHY, RX PHY and TX PLL blocks for data rate switch and PMA analog settings (TX VOD and pre-emphasis). To fulfill the simplex TX and RX PHY channel merging requirement, a transceiver arbiter is inserted in between the Bitec reconfiguration module Avalon-MM master and the PHY reconfiguration Avalon-MM slave interface.

Push Buttons and LEDs

The reference design uses the push buttons and LEDs on the Arria 10 FPGA Development Kit as functional indicators.

Table 7. Push Buttons

Function	Pin Number/ I/O Standard	Schematic Net Name	Reference Designator	Description
Reset	BD27/1.8V	CPU_RESETn	S4	Resets the reference design.
Display MSA values	T12/1.8V	USER_PB0	S3	Display the current TX/RX MSA values and link configuration on the Nios II terminal.

Table 8. LEDs

Function	Pin Number/ I/O Standard	Schematic Net Name	Reference Designator	Description
DisplayPort Sink video locked	L28/1.8V	USER_LED_G0	D10	When illuminated, it indicates that the DisplayPort Sink video output stream to the Clocked Video Input IP core is stable.
DisplayPort Sink lane count	K26/1.8V K25/1.8V L25/1.8V J24/1.8V A19/1.8V	USER_LED_G1 USER_LED_G2 USER_LED_G3 USER_LED_G4 USER_LED_G5	D9 D8 D7 D6 D5	5-bit indicator of the lane count at the DisplayPort Sink. The LED arrangement is {D5, D6, D7, D8, D9}: • 00001 = 1 lane • 00010 = 2 lanes • 00100 = 4 lanes If LED D7 illuminates while other LEDs are off, the lane count at the DisplayPort Sink is 4.
DisplayPort Sink link rate	C18/1.8V D18/1.8V	USER_LED_G6 USER_LED_G7	D4 D3	2-bit indicator of the link rate at the DisplayPort Sink. The LED arrangement is {D3, D4}: • 00 = 1.62 Gbps (RBR) • 01 = 2.70 Gbps (HBR) • 10 = 5.40 Gbps (HBR2) If LED D3 illuminates while LED D4 is off, the DisplayPort Sink is operating at HBR2 link rate.

Reference Design Folders and Files

All the relevant design files reside in the project folder.

Table 9.

Folder/File Name	Description
rtl/core/altera_avalon_i2c	Contains I²C master source files. I²C master is not used in this reference design.
rtl/core/dp_core	Contains the generated IP files and subfolders in dp_core.qsys of the Qsys system.
rtl/core/ip/dp_rx	Contains the generated IP files and subfolders in dp_rx.qsys of the Qsys subsystem *Note:* Only for Quartus® Prime Pro Edition.
rtl/core/ip/dp_tx	Contains the generated IP files and subfolders in dp_tx.qsys of the Qsys subsystem. *Note:* Only for Quartus Prime Pro Edition.
rtl/core/ip/vip	Contains the generated IP files and subfolders in vip.qsys of the Qsys subsystem. *Note:* Only for Quartus Prime Pro Edition.
master_image	Contains precompiled .sof and .elf files.
rtl/rx_phy/gxb_rx	Contains generated RX PHY IP files.
rtl/rx_phy/gxb_rx_reset	Contains generated RX PHY reset controller IP files.
rtl/tx_phy/gxb_tx	Contains generated TX PHY IP files.
rtl/tx_phy/gxb_tx_fpll	Contains generated TX fPLL IP files.
rtl/tx_phy/gxb_tx_reset	Contains generated RX PHY reset controller IP files.
rtl/i2c_gpio_buf	Contains generated IO buffer IP files for the I²C master interface. I²C master is not used in this reference design.
rtl/video_pll_a10	Contains generated IO PLL IP files for video PLL.
software	Contains the Nios II software project. The dp_demo.zip file contains the software project; the dp_demo folder contains the .qip and .hex files of the software project.
tcl	Contains the TCL script for debugging purpose.
software/main.c, software/rx_utils.c, software/tx_utils.c, software/tx_utils.h, software/config.h, and software/vip.h	These are the C source code and header files. You can customize these files for your applications. These files will be copied to the software folder when you run the build_sw.sh script.
top.qpf and top.qsf	The Quartus Prime project and setting files for this reference design.
rtl/core/dp_core.qsys, rtl/core/dp_rx.qsys, rtl/core/dp_tx.qsys, and rtl/core/vip.qsys	The dp_core.qsys file belongs to the top level Qsys system. The dp_rx.qsys file belongs to the DisplayPort RX Qsys subsystem, the dp_tx.qsys file belongs to the DisplayPort TX Qsys subsystem, and the vip.qsys file belongs to the VIP Qsys subsystem. The design includes the dp_rx.qsys, dp_tx.qsys, and the vip.qsys files so that dp_core.qsys loads correctly into Qsys. *Note:* For Quartus Prime Standard Edition designs, do not include the dp_rx.qsys, dp_tx.qsys, and vip.sys files in the top.qsf file to avoid synthesis error.
rtl/rx_phy/gxb_rx.qsys	RX Native PHY instance variant file.
rtl/rx_phy/gxb_rx_reset.qsys	RX Native PHY's transceiver PHY reset controller instance variant file.
rtl/tx_phy/gxb_tx.qsys	TX Native PHY instance variant file.

continued...

Folder/File Name	Description
`rtl/tx_phy/gxb_tx_reset.qsys`	TX Native PHY's transceiver PHY reset controller instance variant file.
`rtl/tx_phy/gxb_tx_fpll.qsys`	TX Native PHY's FPLL instance variant file.
`rtl/i2c_gpio_buf.qsys`	I^{2}C buffer instance variant file. This buffer is not used in this reference design.
`rtl/video_pll_a10.qsys`	IO PLL instance variant file.
`rtl/example.sdc`	Top level SDC timing constraint file.
`script/build_sw.sh`	Shell script to re-build the NIOS II software.
`script/rerun.sh`	Shell script to load the FPGA hardware image (`.sof`) and software image (`.elf`).
`dp_core.sopcinfo`	The `build_sw.sh` script uses this file to rebuild the Nios II software for the control Qsys system.
Others sopcinfo files	These files are not needed to rebuild the Nios II software.
`quartus/dp_vip_xcvr.stp`	SignalTap II file for debug purpose.
`rtl/a10_reconfig_arbiter.sv`	HDL module to arbitrate access to the Avalon-MM interface of the TX and RX Native PHY. This module is needed for merging simplex TX/RX Native PHY into the same physical transceiver channel.
`rtl/mr_rate_detect.v`	HDL module to measure clock frequency.
`rtl/a10_dp_demo.v`	Top-level HDL file for this reference design.
`rtl/bitec_reconfig_alt_a10.v`	HDL module to dynamically reconfigure the TX/RX Native PHY and TX fPLL for data rate switching.
`filelist.txt`	A list of all the files consisting in this design.

Quick Start Guide

The reference design features a hardware design that supports compilation and hardware testing.

Hardware and Software Requirements

To test the reference design, ensure that you have the appropriate hardware and software.

Hardware

- Arria 10 GX FPGA Development Kit (10AX115S2F45I1SG)
- DDR4 HiLo module installed on the development kit
- Bitec FMC daughter card revision 5.0 or later
- 2 DisplayPort cables
- Micro USB cable
- PC with graphic card that supports 3840 × 2160 resolution
- Monitor that supports 3840 × 2160 resolution

Software

- Intel Quartus Prime (for hardware testing)

The reference design is tested with AMD Radeon HD 7700 graphic card, and NVIDIA* NVS* 310 and ASUS* MG28UQ 4K monitors.

Related Information

- Arria 10 DisplayPort 4Kp60 with Video and Image Processing Pipeline Retransmit Reference Design (Quartus Prime Pro Edition)
  Click to get the reference design files using the Quartus Prime 17.0 Pro Edition software. Click on the tabs for other versions.
- Arria 10 DisplayPort 4Kp60 with Video and Image Processing Pipeline Retransmit Reference Design (Quartus Prime Standard Edition)
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- Arria 10 GX FPGA Development Kit
  Refer to this page for more information about the Arria 10 GX FPGA Development Kit.
- FMC DisplayPort Daughter Card

Compiling and Running the Reference Design

Use the provided design files to run the reference design. Intel also provides precompiled `a10_dp_demo.sof` and `dp_demo.elf` files as part of the project file in the `master_image` directory.

Follow these steps to run the reference design:

1. Configure your PC to produce an image at resolution of 1920 × 1080.
2. Install the Bitec FMC daughter card at FMC port A of the development kit.
3. Install the DDR4 HiLo module onto the development kit.
4. Connect the development kit to your PC using a micro USB cable.
5. Connect the DisplayPort cable from your monitor to the TX DisplayPort connector on the FMC daughter card.
6. Connect the DisplayPort cable from your PC to the RX DisplayPort connector on the FMC daughter card.
7. Power up the development kit.
8. Extract the reference design to your PC.
9. Launch the Nios II command shell. Navigate to the `script` directory in the reference design project folder.
10. Load the design into the FPGA by typing `./rerun.sh` at the Nios II command shell.
    a. To use the precompiled `a10_dp_demo.sof` and `dp_demo.elf` files, make sure the files are in the following directory in the `rerun.sh` script:

    ```
    SOPC_DIR=../master_image
    APP_DIR=../master_image
    ```

    b. To use your own compiled `.sof` file and rebuild the `.elf` file, make sure the files are in the following directory in the `rerun.sh` script and the name of the `.sof` file is correct:

    ```
    SOPC_DIR=../quartus
    ```

```
APP_DIR=../software/dp_demo
SOF_NAME=top.sof
```

11. The script loads the `.sof` file, then the `.elf` file and launches the Nios II terminal.

    Note: If you have more than 1 development kit or Intel FPGA Download Cable connected to your PC, you need to type `./rerun.sh<`*`USB cable number`*`>`. To find the cable number, type `jtagconfig` at the DOS command prompt.

12. Extract the `dp_demo.zip` file and place the extracted folders in the software folder. The `dp_demo.zip` file contains the `.hex` file for the Nios II software image. (Optional)

Viewing the Result

The result shows if your design runs correctly.

After you run the design, you should see the image from your PC overlapping with the color bar background.

Note: If you do not see visible output on the monitor, press push button CPU_RESETn (S4) to generate a reset, causing the DisplayPort TX core to retrain the link.

Figure 3. Arria 10 FPGA Development Kit Hardware Setup

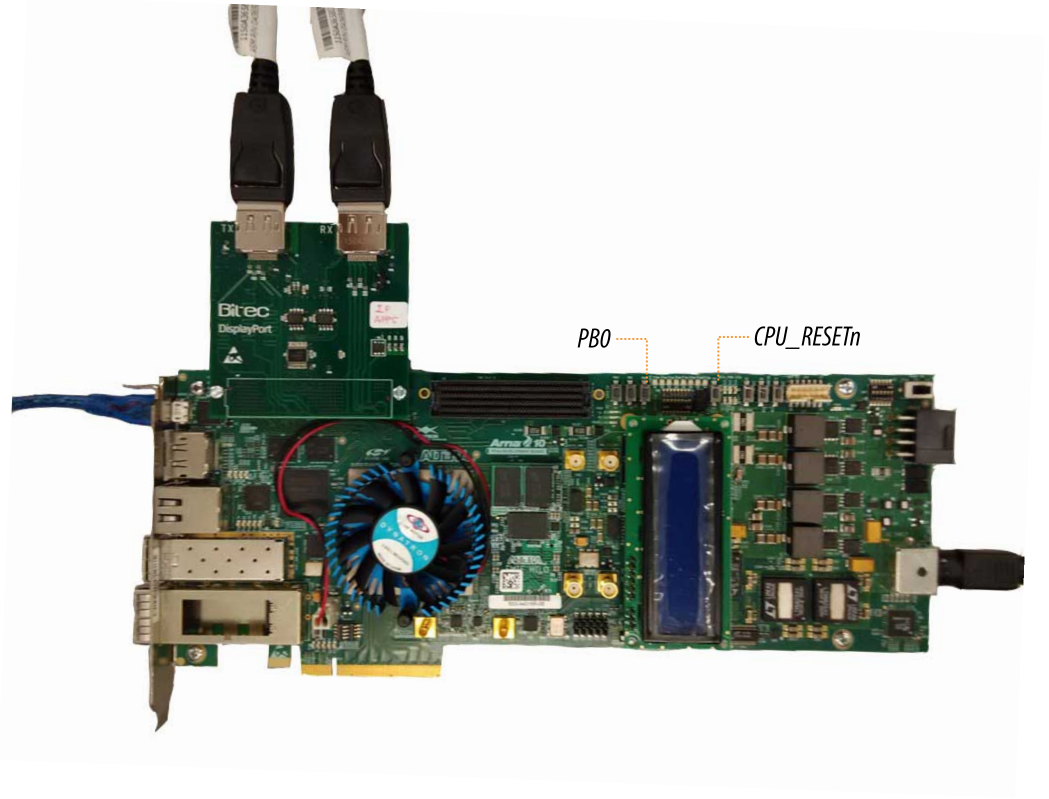
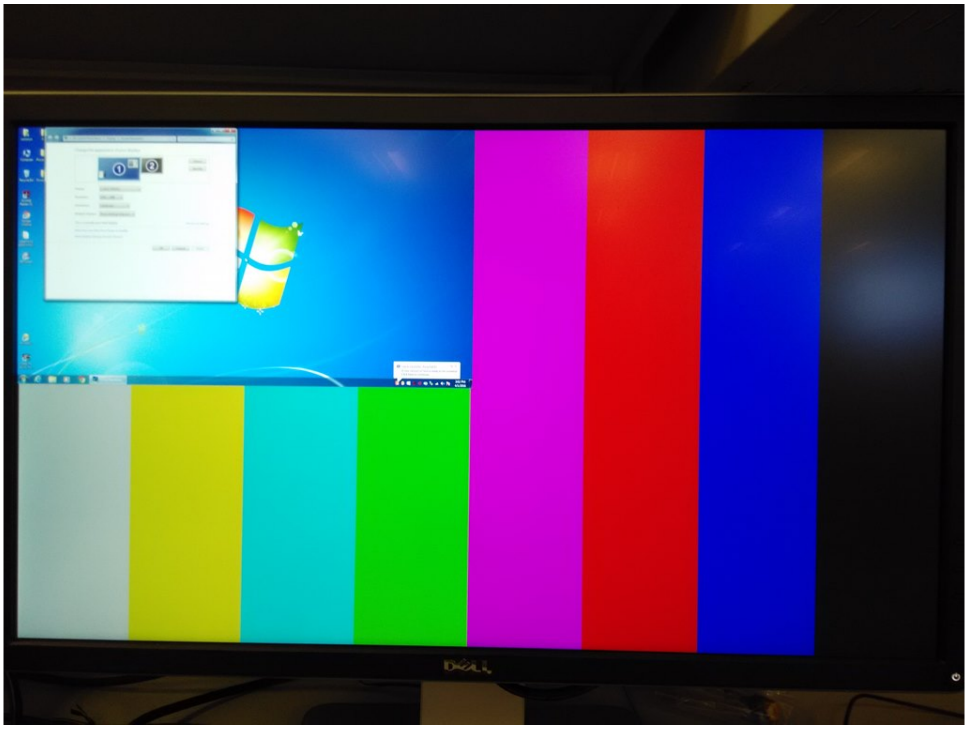
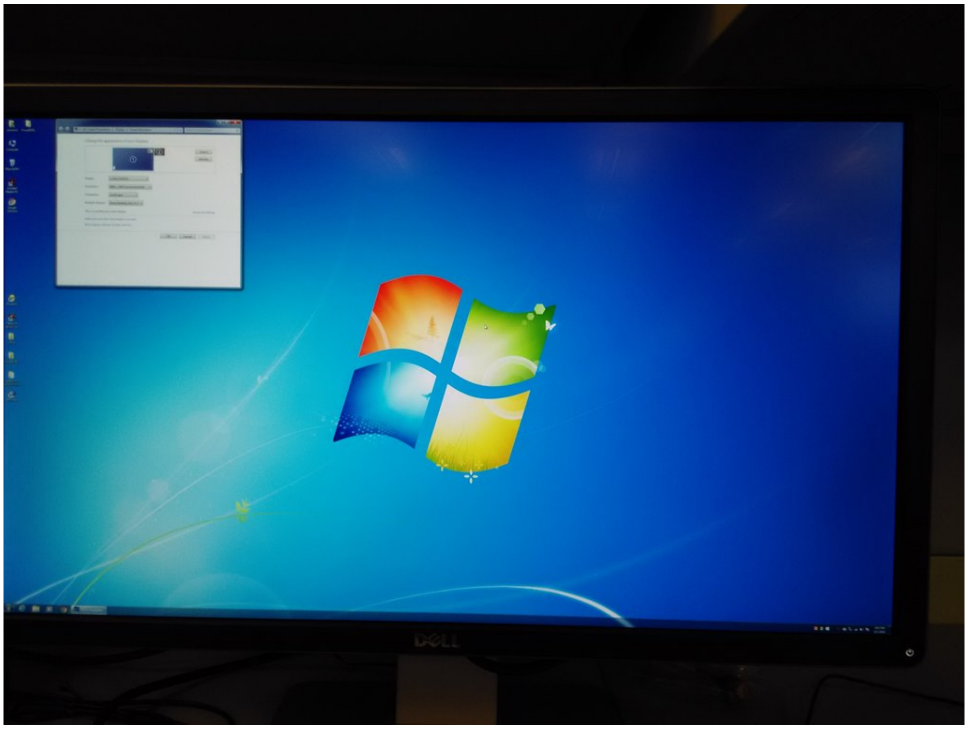


Figure 4. Image from PC Mixed with Color Bar Background



You can scale the image to the maximum resolution of 3840 × 2160. You should see the image getting refreshed on the screen.

Figure 5. No Color Bar Background at 3840 × 2160 Image Resolution



At this resolution, the image from the PC covers the entire color bar background.

Attention: DO NOT scale the resolution beyond 3840 × 2160 to avoid unexpected side effects at the Mixer II output.

The AMD Radeon 7700 and NVIDIA NVS 310 GPUs support certain resolutions with full screen display.

Table 10. Supported Resolutions with Full Screen Display

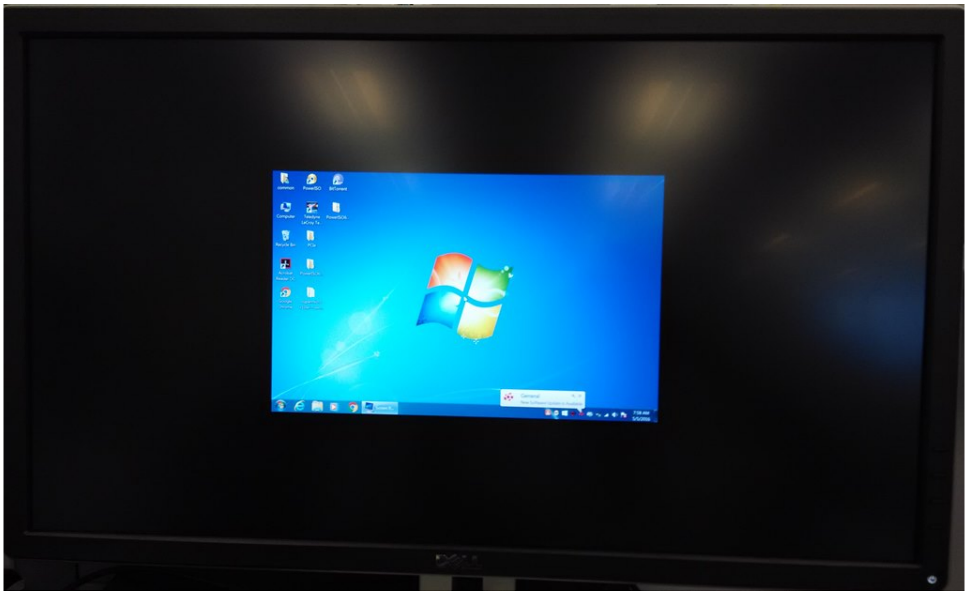
Supported Resolution with Full Screen Display	AMD Radeon HD 7700 GPU	NVIDIA NVS 310 GPU
3840 × 2160	Supported	Supported
2560 × 1660	Supported	Supported
2560 × 1440	Supported	Supported
1920 × 1080	Supported	Supported
1680 × 1050	Supported	Supported
1440 × 900	Supported	–
1280 × 1024	Supported	Supported
1280 × 960	Supported	Supported
1280 × 800	Supported	Supported

continued...

Supported Resolution with Full Screen Display	AMD Radeon HD 7700 GPU	NVIDIA NVS 310 GPU
1280 × 720	Supported	Supported
1024 × 768	Supported	Supported
800 × 600	Supported	Supported

If you configure the GPU to produce images with resolutions other than the ones listed, you may observe a non-full screen display with no color bar background.

Figure 6. No Color Bar Background When Original Image is Not Full Screen



When the image is looped through the FPGA loaded with this reference design, there is no color bar because the GPU transmits the active image and black background at the resolution of 3840 × 2160.

Rebuilding the Nios II Software

If you change the Nios II software, you can rebuild the software using the Nios II command shell.

At the command shell, navigate to the `script` directory in the reference design project folder, and type `./build_sw.sh`.

If you make any changes to the connection or components in the top-level Qsys system (`dp_core.qsys`), DisplayPort RX subsystem (`dp_rx.qsys`), DisplayPort TX subsystem (`dp_tx.qsys`), or VIP subsystem (`vip.qsys`), click **Generate HDL** at the top-level Qsys system and then perform a full compilation.

Because the `sopcinfo` file is updated after the Qsys system is regenerated, you can rebuild the Nios II software while the full compilation is in progress.

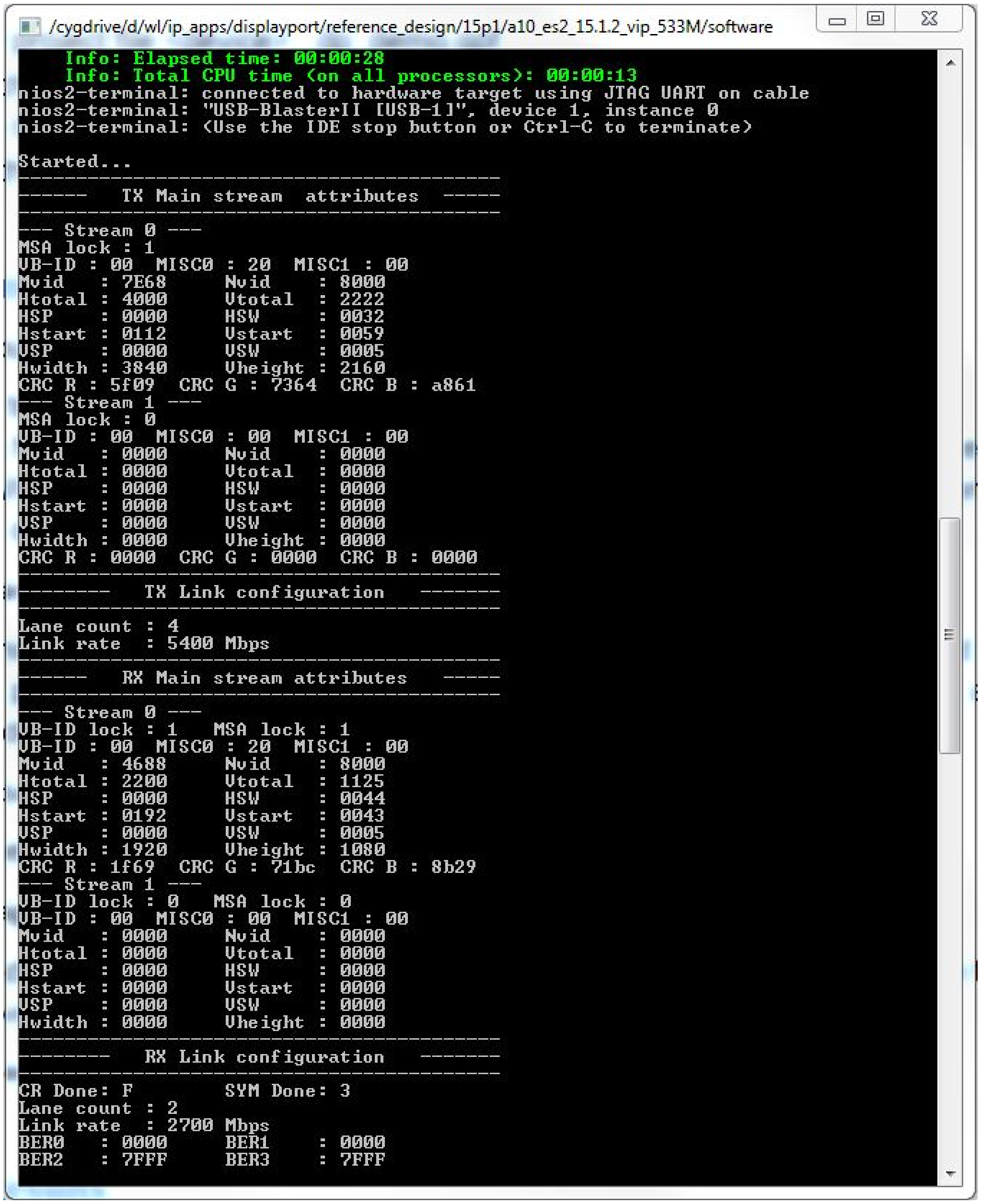
Reference Design Debug Features

There are several debug features in this reference design that are useful for debugging link up and no video output issues.

Main Stream Attribute Info

This debug feature is a part of the DisplayPort IP Core hardware demonstration design example. To display the Main Stream Attribute (MSA) of DisplayPort TX and RX cores, press the PB0 push button (S3) on the development kit. The TX and RX stream MSA values appears on the Nios II terminal.

Figure 7. MSA Values on Nios II Terminal



/cygdrive/d/wl/ip_apps/displayport/reference_design/15p1/a10_es2_15.1.2_vip_533M/software

```
    Info: Elapsed time: 00:00:28
    Info: Total CPU time (on all processors): 00:00:13
nios2-terminal: connected to hardware target using JTAG UART on cable
nios2-terminal: "USB-BlasterII [USB-1]", device 1, instance 0
nios2-terminal: (Use the IDE stop button or Ctrl-C to terminate)

Started...
------------------------------------------
------   TX Main stream  attributes  -----
------------------------------------------
--- Stream 0 ---
MSA lock : 1
VB-ID : 00  MISC0 : 20  MISC1 : 00
Mvid   : 7E68     Nvid     : 8000
Htotal : 4000     Vtotal   : 2222
HSP    : 0000     HSW      : 0032
Hstart : 0112     Vstart   : 0059
VSP    : 0000     VSW      : 0005
Hwidth : 3840     Vheight  : 2160
CRC R : 5f09  CRC G : 7364  CRC B : a861
--- Stream 1 ---
MSA lock : 0
VB-ID : 00  MISC0 : 00  MISC1 : 00
Mvid   : 0000     Nvid     : 0000
Htotal : 0000     Vtotal   : 0000
HSP    : 0000     HSW      : 0000
Hstart : 0000     Vstart   : 0000
VSP    : 0000     VSW      : 0000
Hwidth : 0000     Vheight  : 0000
CRC R : 0000  CRC G : 0000  CRC B : 0000
------------------------------------------
--------   TX Link configuration   -------
------------------------------------------
Lane count : 4
Link rate  : 5400 Mbps
------------------------------------------
------   RX Main stream attributes   -----
------------------------------------------
--- Stream 0 ---
VB-ID lock : 1   MSA lock : 1
VB-ID : 00  MISC0 : 20  MISC1 : 00
Mvid   : 4688     Nvid     : 8000
Htotal : 2200     Vtotal   : 1125
HSP    : 0000     HSW      : 0044
Hstart : 0192     Vstart   : 0043
VSP    : 0000     VSW      : 0005
Hwidth : 1920     Vheight  : 1080
CRC R : 1f69  CRC G : 71bc  CRC B : 8b29
--- Stream 1 ---
VB-ID lock : 0   MSA lock : 0
VB-ID : 00  MISC0 : 00  MISC1 : 00
Mvid   : 0000     Nvid     : 0000
Htotal : 0000     Vtotal   : 0000
HSP    : 0000     HSW      : 0000
Hstart : 0000     Vstart   : 0000
VSP    : 0000     VSW      : 0000
Hwidth : 0000     Vheight  : 0000
------------------------------------------
--------   RX Link configuration   -------
------------------------------------------
CR Done: F        SYM Done: 3
Lane count : 2
Link rate  : 2700 Mbps
BER0   : 0000     BER1     : 0000
BER2   : 7FFF     BER3     : 7FFF
```

Auxiliary Channel Traffic Monitor

This debug feature is also a part of the DisplayPort IP core hardware demonstration design example. To display the auxiliary channel transaction on the Nios II terminal, set the BITEC_AUX_DEBUG flag in `config.h` in the project folder to 1.

```
#define BITEC_AUX_DEBUG 1 // Set to 1 to enable AUX CH traffic monitoring
```

Rebuild the Nios II software and download the ELF image into the FPGA.

Logic Analyzer

If you want to monitor the Avalon-ST stream of the Clocked Video Input II, Clocked Video Output II, and Mixer II signals, recompile this reference design by enabling the SignalTap II Logic Analyzer using `dp_vip_xcvr.stp`. This STP file also includes a list of clocked video signals of DisplayPort sink–Clocked Video Input II, DisplayPort source–Clocked Video Output II, and DisplayPort–transceiver interfaces.

You can monitor the TX and RX recovered clock frequency by reading the values at the `refclock_measure` ports in the `mr_rate_detect.v` module.

System Console

The top level Qsys includes a JTAG to Avalon Master Bridge.

- The TCL script in the `tcl` folder allows you to control the operation of the VIP IP cores.
- The `main.tcl` script contains the procedures to access the Clocked Video Input II, Clocked Video Output II, Mixer II, and Frame Buffer II control and status registers.
- The `vip_csr_offset.tcl` file contains the CSR offset of the Clocked Video Input II, Clocked Video Output II, Mixer II, and Frame Buffer II IP cores.
- The `system_base_addr_map.tcl` contains the Qsys base address of these VIP IP cores.

In this reference design, the system console accesses the Mixer CSR through the Avalon-MM interface. To access the CSR of other VIP IP cores:

1. Drill into the VIP Qsys subsystem and enable the CSR Avalon-MM interface of the IP core.
2. Connect the control port (Avalon-MM slave) to the m0 port of the Avalon-MM Pipeline Bridge component, `mm_bridge_vip`.

When assigning the base address in the VIP Qsys subsystem of the Avalon-MM slave of the VIP IP cores, follow the address map in the `system_base_addr_map.tcl` file:

- Clocked Video Input II: 0x0000
- Mixer II: 0x0200
- Clocked Video Output II: 0x0400
- Frame Buffer II: 0x0800

In `dp_core.qsys`, open the `Address Map` tab, and ensure the base address for connecting `master_0.master` and `vip.mm_bridge_vip_s0` starts from 0x0000.

Move up to the top-level Qsys from VIP subsystem, regenerate the Qsys and perform a full compilation. To have full control of the VIP IP cores CSR, (e.g. to debug no video output issue), stop the Nios II processor from accessing the CSR.

1. Clear the ALT_VIP flag in `config.h`:

   `#define ALT_VIP 0` // Set to 1 if a VIP IP core (e.g. Mixer II) is used
2. Rebuild the Nios II software and program the updated ELF file.
3. Launch the system console and type these commands to load the `main.tcl` file and display the Mixer II output:

```
cd tcl
source main.tcl
go
```

Note: You may need to modify the `master_index` variable in the `main.tcl` file to access the correct service path.

4. To stop the Mixer II from displaying video stream at its input 0 port and display the color bar only, type

```
mixer_input0_stop
```

Known Issues

Warning Message in Windows

You may observe a DisplayPort Link Failure message when using GPU with other than the AMD Radeon HD 7700 GPU and ASUS MG28UQ 4K monitors. Adjust the resolution and refresh rate to match the capability of your monitor.

Revision History

Date	Version	Changes
June 2017	2017.06.13	• Edited the reference design block diagram to reflect the updated reference design. • Edited the files and folders based on the updated reference design. • Changed DDR3 to DDR4. The updated reference design uses DDR4 running at 1066 MHz. • Updated the information on the required monitors for testing. The updated reference design is tested with AMD Radeon HD 7700 graphic card, and NVIDIA NVS 310 and ASUS MG28UQ 4K monitors. • Changed the reset to CPU_RESETn based on the updated reference design. • Added additional information about the VIP IP core parameters. • Updated the supported resolution with full screen display information for the monitors.
December 2016	2016.12.28	Initial release.